

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:
a semiconductor substrate;
a lowermost layer nearest to said semiconductor
5 substrate;

an uppermost layer farthest from said
semiconductor substrate; and

intermediate layers arranged between said
lowermost layer and said uppermost layer;

10 wherein when one of said intermediate layers is
set as a first intermediate layer and the other one
of said intermediate layers is set as a second
intermediate layer, said first intermediate layer is on
said lowermost layer side compared with said second
15 intermediate layer and said first intermediate layer is
thicker than said second intermediate layer.

2. The semiconductor device according to claim 1,
wherein a wiring pitch of said first intermediate
layer is wider than a wiring pitch of said second
20 intermediate layer.

3. The semiconductor device according to claim 1,
wherein said first intermediate layer is a layer on
which a power source line is formed.

4. The semiconductor device according to claim 1,
25 wherein said first intermediate layer comprises a first
area having signal lines and a second area having power
source lines, and a pitch of said power source lines is

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wider than that of said signal lines.

5 5. The semiconductor device according to claim 1,
wherein said first intermediate layer comprises a first
area having signal lines and a second area having power
source lines, and a width of each of said power source
lines is wider than that of said signal lines.

6. The semiconductor device according to claim 1,
wherein said first intermediate layer is substantially
as thick as said uppermost layer.

10 7. The semiconductor device according to claim 1,
wherein said second intermediate layer is substantially
as thick as said lowermost layer.

8. The semiconductor device according to claim 1,
wherein all of said uppermost layer, said lowermost
15 layer and said intermediate layers are metal layers.

9. A semiconductor device comprising:
a semiconductor substrate;
an IP core area on said semiconductor substrate;
a peripheral area on said semiconductor substrate
20 except for said IP core area;

a lowermost layer nearest to said semiconductor
substrate;

an uppermost layer farthest from said
semiconductor substrate; and

25 intermediate substrates arranged between said
lowermost layer and said uppermost layer;

wherein when one of said intermediate layers is

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set as a first intermediate layer and the other one of
said intermediate layers is set as a second
intermediate layer, said first intermediate layer is on
said lowermost layer side compared with said second
intermediate layer and said first intermediate layer is
thicker than said second intermediate layer.

10. The semiconductor device according to claim 9,
wherein said uppermost layer and all the intermediate
layers between said first intermediate layer and said
uppermost layer are formed only in said peripheral
area, and said first intermediate layer is an uppermost
layer farthest to said semiconductor substrate in said
IP core area.

11. The semiconductor device according to
claim 10, wherein said first intermediate layer is
a layer on which a core power source line is formed in
said IP core area.

12. The semiconductor device according to claim 9,
wherein a wiring pitch of said first intermediate layer
is wider than a wiring pitch of said second
intermediate layer.

13. The semiconductor device according to claim 9,
wherein said first intermediate layer is substantially
as thick as said uppermost layer.

14. The semiconductor device according to claim 9,
wherein said second intermediate layer is substantially
as thick as said lowermost layer.

15. The semiconductor device according to claim 9,
wherein said first intermediate layer comprises a first
area having signal lines and a second area having power
source lines, and a pitch of said power source lines is
5 wider than that of said signal lines.

16. The semiconductor device according to claim 9,
wherein said first intermediate layer comprises a first
area having signal lines and a second area having power
source lines, and a width of each of said power source
10 lines is wider than that of said signal lines.

17. The semiconductor device according to claim 9,
wherein all of said uppermost layer, said lowermost
layer and said intermediate layers are metal layers.

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